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⑭発明の名称　記憶システム

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明　細　書

1．発明の名称

記憶システム

2．特許請求の範囲

(1) 主記憶装置と該主記憶装置のアクセス制御を行う記憶制御装置とからなる記憶システムにおいて、前記主記憶装置と記憶制御装置に共通のクロック線を設けると共に、前記主記憶装置は、該主記憶装置内のメモリ素子の動作特性を示す情報を格納する手段と、前記クロック線を使用してメモリ素子の制御信号、読書きデータのセット信号等を生成する手段と、これらの信号を前記情報に基いて可変とする手段を備えていることを特徴とする記憶システム。

3．発明の詳細な説明

〔産業上の利用分野〕

本発明は主記憶装置とそのアクセス制御を行う記憶制御装置よりなる記憶システムに係り、特に、高速アクセス制御を容易にし、しかも処理装置やメモリ素子の変動に対して柔軟性を与えるのに好適な記憶システムに関する。

〔従来の技術〕

従来の電子計算機においては、例えば特開昭57－101957号公報の記載のように、主記憶装置は、該主記憶装置（以下MSと略す）を制御する記憶制御装置（以下SCUと略す）あるいはSCUより命令やデータを受取って実行する命令プロセッサ（以下IPと略す）で使用するクロックに対し、独立のクロックを保持していた。これは、MSのクロックは、MSで使用するRAM等の記憶素子の動作仕様によって決定されることによる。

SCUとMS間のインタフェースの制御では、SCUがMSに対して起動信号とアクセスの種別を示した信号を送出し、MSでの処理が終了すると、MSはSCUに対して終了報告を行っている。他には、SCUがMSの処理の時間管理を行う方法がある。これは、SCUがMSに対し起動信号を送出した後、アクセスの種別により、時間設定をSCUでカウントし、一定時間が経過すると、

ＳＣＵからＭＳに対して、データ送出等の指示をする信号を送出して、管理する方法である。

一方、ＳＣＵ、ＩＰの処理速度、つまりマシンサイクルを可変にしたり、あるいは動作仕様の異なるＭＳを接続したりすることがある。この時、上記、ＳＣＵがＭＳを管理する方法を取る場合、時間設定情報をＳＣＵ内に保持し、ＳＣＵとＭＳのインタフェースを可変として対処する方法等が考えられている。

〔発明が解決しようとする問題点〕

最近、連続してデータの読出し、書込みを高速に行うことが可能なメモリ素子が開発されている（例えば、ニブルモードとか高速ページモード）。また、装置で使用されるデバイス技術の進歩により、より高速にＭＳをアクセスする技術が現れている。　しかしながら、上記従来技術のように、ＳＣＵとＭＳにおいて別々のクロックを備えている場合、上記高速メモリ素子を使用して高速にアクセスしようとしても、ＳＣＵとＭＳが非同期のため、制御が困難であるという問題があった。

クルピッチで行うことが可能となり、書込みの場合は、ＳＣＵ内のラッチからＭＳのラッチへデータを何サイクルピッチで送出し、これをメモリ素子へ書込むことが可能となる。さらに、上記信号を種々の位相、サイクル数で送出できるようにすることにより、マシンサイクル、あるいはメモリ素子の動作仕様に適合した信号を選択でき、使用するメモリ素子に柔軟性を与えることが可能となる。

〔実施例〕

以下、本発明の一実施例について図面により説明する。

図１図は本発明の一実施例のブロック図を示す。１は命令プロセッサ（ＩＰ）、２は入出力プロセッサ（ＩＯＰ）、３はＳＣＵ、４はＭＳ、５はＩＰ１、ＩＯＰ２、ＳＣＵ３、ＭＳ４へタイミング信号を送出するクロック部である。

１０はＩＰ１からのリクエストを受けるリクエストスタック（ＩＰＲＱ）、１１はＩＯＰ２からのリクエストを受けるリクエストスタック（ＩＯ

本発明の目的は、高速にメモリをアクセスすることが可能で、さらに、マシンサイクルの変動、あるいは動作仕様の異なるメモリ素子の接続に対して柔軟性がある記憶システムを提供することにある。

〔問題点を解決するための手段〕

上記目的は、ＳＣＵとＭＳのクロックを共通化し、ＭＳのメモリ素子を制御する信号、あるいは、データをセットする信号等を上記クロックを使用して生成するとともに、上記各信号をマシンサイクルあるいはメモリ素子の動作仕様を示す情報により可変とする手段をＭＳ内に設けることにより達成される。

〔作　用〕

ＭＳ内のメモリ素子の制御信号、データのセット信号等を、ＳＣＵと同じクロックを使用して、生成することにより、ＳＣＵとの同期化回路が不要になる。従って、読出しの場合は、メモリ素子からデータが出力され、これをＭＳ内ラッチにセットし、ＳＣＵ内ラッチへ送出する動作を何サイ

ＰＲＱ）、１２はＩＰ１からのストアデータを受取るデータラッチ（ＩＰＳＤ）、１３はＩＯＰからのストアデータを受取るデータラッチ（ＩＯＰＳＤ）である。１４はＭＳ４から読出したデータをラッチし、ＩＰ１あるいはＩＯＰ２へ送出するデータラッチ（ＳＦＤ）である。１５はＭＳ４へストアデータを送出するためのストアデータラッチ（ＳＳＤ）、１６はＭＳ４へＳＣＵ３のリクエストを送出するためのラッチ（ＳＲＱ）である。５０はＳＣＵ３を制御するＳＣＵコントロールユニット（ＳＣＲ）である。

２０はＳＲＱ１６から送られたリクエストをＭＳ４で受取るラッチ（ＭＲＱ）、２１はＳＳＤ１５から送られたストアデータをＭＳ４で受取るストアデータラッチ２１（ＭＳＤ）である。２２～２５は後述するメモリ素子の集合体に各々備えられたストアデータラッチ（ＳＤＲ０～３）、２６～２９は同じくフェッチデータラッチ（ＦＤＲ０～３）である。３０はＳＣＵ４へフェッチデータを送出するためのラッチ（ＭＦＤ）である。４０

に入力される。これにより、カウンタ３００の出力は、デコーダ３０１でデコードされ、Ｃ０～Ｃ３（３０６～３０９）の示す情報により、セレクタ３１４でセレクトされる。例えばＣ０＝"１"であれば、０サイクル目にセレクタ３１４から"１"が出力され、Ｃ１＝"１"であれば、１サイクル目にセレクタ３１４から"１"が出力される。セレクタ３１４の出力は、Ｔ０位相のＦＦ３０２に入力されると同時に、ＳＲＦＦ３１８をリセットする。これにより、カウンタ３００は、カウントアップを止める。Ｔ０～Ｔ３（３１０～３１３）の示す情報により、どの位相で出力するかをセレクタ３１５でセレクトする。この信号をＮＯＴゲート３１７で負論理にする。これは一般に$\overline{RAS}$，$\overline{CAS}$は、負論理でメモリ素子に与えられるためである。ＣＡＳＲＥＳＥＴ信号がＳＲＦＦ３１９に入力されると、ＳＲＦＦ３１９の出力は"０"となり、デコーダ３０１のイネーブル入力は"０"となり、デコーダ３０１の出力は全て"０"となるため、$\overline{CAS}$の出力も"０"となる。

以上説明したように、本発明によれば、ＳＣＵとＭＳで、同じクロックを使用したことにより、ＳＣＵとＭＳ間で同期合せが必要なくなり、高速なメモリ素子を使用した時でも制御が簡単になり、ＭＳを高速にアクセスすることが可能となる。また、ＭＳにメモリ素子の制御信号等を任意のサイクル数、位相で送出できる手段を備えることにより、マシンサイクルの異なや、異なった動作仕様のメモリ素子の接続に対して柔軟性を与える効果がある。

4．図面の簡単な説明

第１図は本発明の一実施例のブロック図、第２図は第１図の動作を説明するタイムチャート、第３図は第１図のＭＳコントローラ内で実施される回路の具体的構成図、第４図は第３図の回路を使用して異なるマシンサイクルのメモリ素子に適合した時のタイムチャートである。

１…命令プロセッサ（ＩＰ）、

２…入出力プロセッサ（ＩＯＰ）、

３…記憶制御装置（ＳＣＵ）、

このようにして、信号を任意のサイクル数、任意の位相で、出力することができる。

第４図はマシンサイクルが異なるＳＣＵに同じ動作仕様のメモリ素子を接続する時、第３図で示す回路構成を利用して$\overline{CAS}$信号を生成する場合のタイムチャートを示したものである。第４図で４００，４０２は$\overline{RAS}$、４０１，４０３は$\overline{CAS}$を示しており、第４図（ｂ）のマシンサイクルは、第４図（ａ）の２倍としている。一般に$\overline{RAS}$から$\overline{CAS}$のディレータイムＴＲＣＤは、メモリの動作仕様として定められており、従ってマシンサイクルが変更しても、ＴＲＣは同じ長にしなければならない。第４図（ａ）では、$\overline{CAS}$信号４０１を、第３図のＣ３（３０９）＝"１"、Ｔ０３１０＝"１"にすることにより、図の通りのタイムチャートとなり、第４図（ｂ）では、$\overline{CAS}$信号４０３を第３図のＣ１（３０７）＝"１"、Ｔ２（３１２）＝"１"と設定することにより、図の通りのタイムチャートが得られる。

（発明の効果）

４…主記憶装置（ＭＳ）、　５…クロック線、

５０…ＳＣＵコントロールユニット、

５１…ＭＳコントロールユニット。

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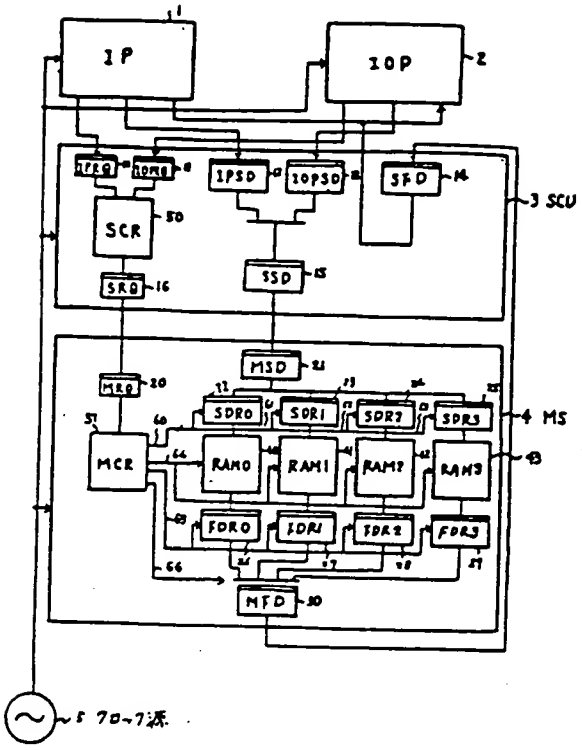
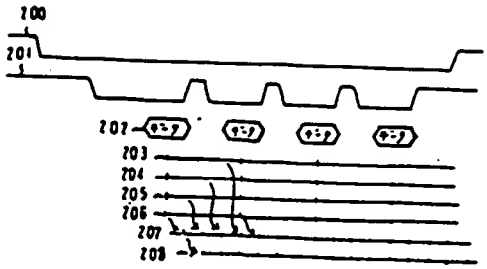
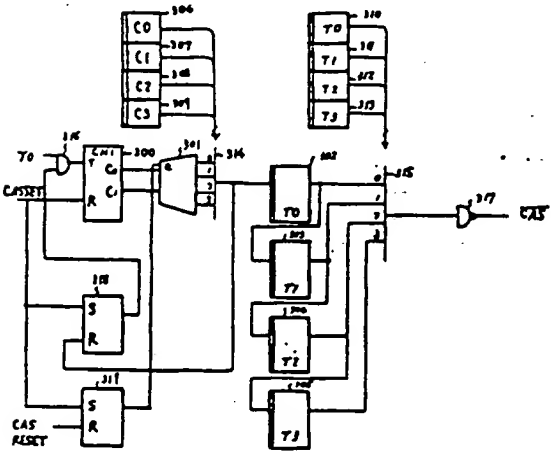
第 1 図



第 2 図

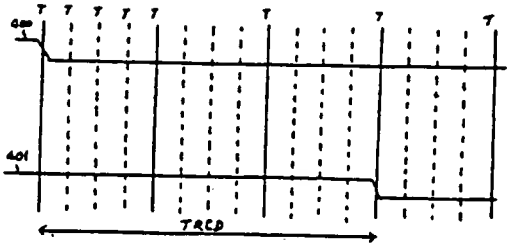


第 3 図

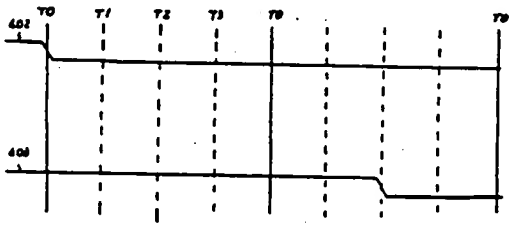


第 4 図

(a)



(b)



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(54) Title of the Invention: Storage system

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Specification

1. Title of the Invention

Storage System

2. Claims

(1) In a storage system consisting of a main storage unit and a storage control unit that carries out the access control of said main storage unit, a storage system characterized by the fact that a clock source common to the main storage unit and the storage control unit mentioned above is provided, and, in addition, the above-mentioned main storage unit is provided with a means that stores the information that shows the operation characteristics of a memory device inside of said main storage unit, and a means that generates a memory device control signal that uses the above-mentioned clock source, a read/write data set signal, and the like, and a means that regards these signals based on the above-mentioned information as varying.

3. Detailed Description of the Invention

(Field of Industrial Application)

The present invention is related to a storage system formed from a main storage unit and a storage control unit that carries out its access control and, particularly, is related to a storage system that makes high speed access control easy and, moreover, is suitable for affording flexibility with respect to the fluctuations of a processing unit and memory device.

(Prior Art)

In former computers, for example, as described in Kokai No. S57-101957, the main storage unit maintained independent clocks, with respect to the clocks used by the storage control unit (hereafter referred to as the SCU) that controls said main storage unit (hereafter referred to as the MS) or the instruction processor (hereafter referred to as the IP) that receives data and instructions from said SCU and executes. As for this, the MS clock is determined by the operation specifications of the storage device of the RAM, and the like, used by the MS.

In the control of the interface between the SCU and the MS, the SCU sends to the MS the activation signal and the signal that indicates the type of access, and when the processing by the MS is completed, the MS carries out a completion report with respect to the SCU. In addition to this, the SCU has a method for carrying out the time management of the processing of the MS. This is a control method that, after the SCU has sent an activation signal to the MS, counts the passage of time by the SCU, based on the type of access, and, when a set time has elapsed, sends from the SCU to the MS a signal that directs data sending, and the like.

On the other hand, sometimes the processing speed, that is, the machine cycles, of the SCU and the IP is made variable, or an MS with different operation specifications is connected. At this time, the above-mentioned, when the SCU adopts a method that

controls the MS, holds in the SCU the time specification information and a method, and the like, that handles the interface of the SCU and the MS as variable can be thought of.

(Problem the Invention is to Solve)

Recently, memory devices that can carry out the reading and writing of linked data at a high speed are being developed (for example, the nibble mode and the high-speed page mode). Furthermore, due to the advance of device technology used by logic, technology that accesses the MS at a still higher speed is desirable. However, as in the above-mentioned prior art, when separate clocks were provided in the SCU and the MS, there was the problem that even when access at a high speed is attempted using the above-mentioned high-speed memory device, because the SCU and the MS are unsynchronized, control is difficult.

The purpose of the present invention is to offer a storage system that makes possible accessing memory at a high speed, and, moreover, that has flexibility with respect to the fluctuation of machine cycles, or the connection of memory devices with different operation specifications.

(Means for Solving the Problem)

The above-mentioned purpose is achieved due to the fact that the clocks of the SCU and the MS are made to be in common, and the above-mentioned clocks are used and generate the signal that controls the memory device of the MS, or the signal that sets the data, and the like, and, in addition, a means that makes each of the above-mentioned signals variable by means of machine cycles or information that sets forth the operation specification of the memory device is provided within the MS.

(Operation)

A circuit that synchronizes with the SCU becomes unnecessary due to the fact that the same clock as that of the SCU is used and generates the control signal of the memory device within the MS and the signal that sets the data, and the like. Consequently, in the case of reading, data is sent from the memory device, and this is set to a latch within the MS, and carrying out with every cycle pitch the operation that sends to a latch within the SCU becomes possible, and in the case of writing, from a latch within the SCU data is sent with every cycle pitch to a latch of the MS, and writing this to the memory device becomes possible. Furthermore, due to the fact of being made so that the above-mentioned signals can be sent in various phases and cycles, a signal adjusted to the machine cycles or the operation specifications of a memory device can be selected, and affording flexibility to the memory device used becomes possible.

(Embodiment)

Below one embodiment of the present invention is explained based on the drawings.

FIG. 1 shows a block diagram of one embodiment of the present invention. 1 is the instruction processor (IP). 2 is the input/output processor (IOP). 3 is the SCU. 4 is the MS. 5 is the clock source that sends timing signals to the IP 1, the IOP 2, the SCU 3 and the MS 4.

10 is the request stack (IPRQ) that receives a request from the IP 1. 11 is the request stack (IOPRQ) that receives a request from the IOP 2. 12 is the data latch (IPSD) that receives storage data from the IP 1. 13 is the data latch (IOPSD) that receives storage data from the IOP. 14 is the data latch (SFD) that latches the data read from the MS 4 and sends to the IP 1 or the IOP 2. 15 is the storage data latch (SSD) for sending storage data to the MS 4. 16 is the latch (SRQ) for sending the requests of the SCU 3 to the MS 4. 50 is the SCU control unit (SCR) that controls the SCU 3.

20 is the latch (MRQ) that receives at the MS 4 the requests sent from the SRQ 16. 21 is the storage data latch (MSD) that receives at the MS 4 the storage data sent from the SSD 15. 22 ~ 25 are the storage data latches (SDR 0 ~ 3) respectively provided to the array of memory devices described later. 26 ~ 29, similarly, are the fetch data latches (FDR 0 ~ 3). 30 is the latch (MFD) for sending fetch data to the SCU 4. 40 ~ 43 is an array (RAM 0 ~ 3) of memory devices that has arranged the memory devices so as to have the same bit width as the respective latches of SDR 0 ~ 3 (22 ~ 24) and FDR 0 ~3 (26 ~ 29). 51 is the MS control unit (MCR) that controls the MS. 60 ~ 63 are the set signals that set, respectively, SDR 0 ~ 3 (22 ~ 24). 64 is the signal that controls RAM 0 ~ 3. 65 is the signal that sets FDR 0 ~ 3 (26 ~ 29). 66 is the select signal for which data to select of the latches of FDR 0 ~ 3 (26 ~ 29).

The SCU 3 and the MS 4 use the same clock source 5. Signals 60 ~ 63 as well as 65 that set each latch within the MS 4, signal 64 that controls RAM 0 ~ 3, and control signal 66 within the MS 4 all use this clock source 5 and are generated. Consequently, a circuit to carry out synchronization of the SCU 3 and the MS 4 is not necessary at all.

Next, the operation of FIG. 1 is explained with reference to the time chart of FIG. 2. The time chart of FIG. 2 shows the case of the read operation. In FIG. 2, 200 and 201 are included in the control signal 64 of FIG. 1, and show $\overline{\text{RAS}}$, $\overline{\text{CAS}}$. The present time chart shows the operation of the generally known nibble mode. That is, when an address is once given to memory by $\overline{\text{RAS}}$ 200 and $\overline{\text{CAS}}$ 201, after that, simply by the toggling of $\overline{\text{CAS}}$ 201, the data of consecutive addresses can be accessed at a high speed. 202 shows the data output of the RAM 0 ~ 3 (40 ~ 43) of FIG. 1. 203 ~ 206 show the state of the FDR 0 ~ 3 (26 ~ 29) of FIG. 1. Similarly, 207 shows the MFD 30 of FIG. 1, and 208 shows the state of the SFD 14.

The SCU 3 stacks requests from the IP 1 and the IOP 2 in the IPRQ 10 and the IOPRQ 11. The priorities of these requests are taken by the SCR 50, one request is selected and set in the SRQ 16, and sent to the MS 4 side. The MS 4, when a request from the SCU 3 is received by the MRQ 20, by means of the MCR 51, generates a control signal 64 in response to the request. In the example of FIG. 2, $\overline{\text{RAS}}$ 200, $\overline{\text{CAS}}$ 201 are generated as in the drawing. When the RAM 0 ~ 3 (40 ~ 43) is accessed at the same time and the data is output (202), by means of the set signal 65, data simultaneously read is set (203 ~ 206) to the FDR 0 ~ 3 (26 ~ 29). Next, data is transferred (207) by one machine cycle pitch to MFD 30 by means of the select signal 66. When all the data in the latches of FDR 0 ~ 3 (26 ~ 29) have been transferred to the MFD 30, by means of the $\overline{\text{CAS}}$ signal 2201 [sic.], the data of consecutive addresses is read, and again set to FDR 0 ~ 3 (26 ~ 29). Done in this way, reading consecutive data at a high speed by 1 machine cycle

pitch is possible. The data of the MFD 30, similarly, is transferred (208) to the SFD 14F of the SCU 3 by 1 machine cycle pitch.

FIG. 3 shows the detailed constitution of one part inside the MCR 51 of FIG. 1. 300 is a 2 bit counter. 301 is a decoder. 302 is a flip-flop (FF) that sends a signal by the timing of T 0. Similarly, 303 ~ 305 are the FF of the timing of T 1 ~ T 3, respectively. 306 ~ 309 are latches (C 0 ~ C 3) that store the information that shows the number of cycles. 310 ~ 313 are latches (T 0 ~ T 3) that store the information that shows the phase of the clock. 314, 315 are selectors. 316 is an AND gate. 317 is a NOT gate. 318 ~ 319 are FF of a set-reset type (SR).

This place is regarded as that which generates the signal of $\overline{CAS}$ 201 of FIG. 2. When the CASSET signal is input to SRFF 318 and 319, SRFF 318 and 319 are set to "1" and the CASSET signal simultaneously resets the counter 300. When SRFF 318 is set to "1", this output is input to the AND gate 316, and with the next T 0 timing, is input to the T input of counter 300, and +1 is counted up. At the same time, the output of SRFF 319 is input to the enable input of the decoder 301. By means of this, the output of the counter 300 is decoded by the decoder 301, and selected by the selector 314 based on the information shown by C 0 ~ C 3 (306 ~ 309). For example, if it is C 0 = "1", "1" is output from the selector 314 in the 0 cycle, and, if C 1 = "1", "1" is output from the selector 314 in the first cycle. The output of selector 314, at the same time as being input to the FF 302 of the T 0 phase, resets the SRFF 318. By means of this, the counter 300 stops counting up. Based on the information shown by T 0 ~ T 3 (310 ~ 313), which phase to output at is selected by the selector 315. This signal is made negative logic by the NOT gate 317. This, generally, is because $\overline{RAS}$, $\overline{CAS}$ are given to a memory device by negative logic. When the CASRESET signal is input to the SRFF 319, because the output of the SRFF 319 becomes "0", and the enable input of the decoder 301 becomes "0", and the output of the decoder 301 all becomes "0", the output of $\overline{CAS}$ also becomes "0".

Done in this way, a signal can be output at any number of cycles and any phase.

FIG. 4 shows the time chart when the $\overline{CAS}$ signal is generated using the circuit configuration shown by FIG. 3, when memory devices with the same operation specifications are connected to SCU with different machine cycles. In FIG. 4, 400 and 402 show the $\overline{RAS}$, and 401 and 403 show the $\overline{CAS}$, and the machine cycles of FIG. 4 (b) are regarded as double those of FIG. 4 (a). Generally, the delay time TRCD of the $\overline{CAS}$ from the $\overline{RAS}$ is provided as the operation specification of the memory, consequently, even if the machine cycles fluctuate, the TRC must be made the same value. In FIG. 4 (a), by making the $\overline{CAS}$ signal 401 the C 3 (309) = "1" and the T 0 310 = "1" of FIG. 3, the time chart as in the drawing is formed, and in FIG. 4 (b), by setting the $\overline{CAS}$ signal 403 to the C 1 (307) = "1" and the T 2 (312) = "1" of FIG. 3, a timing chart as in the drawing can be obtained.

(Effect of the Invention)

As explained above, according to the present invention, due to the fact that the same clock is used by the SCU and the MS aligning the synchronicity between of the SCU and

the MS becomes unnecessary, and control becomes simple even when a high speed memory device is used, and accessing the MS at a high speed becomes possible. Furthermore, there is the effect that, due to the fact that a means that can output to the MS a control signal, and the like, of a memory device at any number of cycles and phase, flexibility is given with respect to the fluctuations of the machine cycle and the connection of a memory device with a different operation specification.

4. Brief Description of the Drawings

FIG. 1 is a block diagram of one embodiment of the present invention. FIG. 2 is a time chart that explains the operation of FIG. 1. FIG. 3 is a diagram of a specific constitution of the circuit implemented within the MS controller of FIG. 1. FIG. 4 is a time chart of the time when the circuit of FIG. 3 is used and a memory device of different machine cycles has been adapted to.

1 Instruction processor (IP)

2 Input/Output processor (IOP)

3 Storage control unit (SCU)

4 Main storage unit (MS)

5 Clock source

50 SCU control unit

51 MS control unit

Agent Makoto Suzuki, Patent Attorney [seal]

FIG. 1

5 clock source

FIG. 2

202 data data data data

FIG. 3

FIG. 4